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Relevance scale

1 Embedded software: task scheduling and compilation: Data partitioning for maximal scratchpad usage
Manish Verma, Stefan Steinke, Peter Marwedel
January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**
Publisher: ACM Press
Full text available: pdf(118.25 KB) Additional Information: full citation, abstract, references

The energy consumption for Mobile Embedded Systems is a limiting factor because of today's battery capacities. The memory subsystem consumes a large chunk of the energy, necessitating its efficient utilization. Energy efficient scratchpads are thus becoming common, though unlike caches they require to be explicitly utilized. In this paper, an algorithm integrated into a compiler is presented which analyzes the application, partitions an array variable whenever its beneficial, appropriately modif ...

2 Session 3C: Routing architecture and techniques for FPGAs: A search-based bump-and-refit approach to incremental routing for ECO applications in FPGAs
Vinay Verma, Shantanu Dutt
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(198.08 KB) Additional Information: full citation, abstract, references, index terms

Incremental physical CAD is encountered frequently in the so-called engineering change order (ECO) process in which design changes are made typically late in the design process in order to correct logical and/or technological problems in the circuit. As far as routing is concerned, in order to capitalize on the enormous resources and time already spent on routing the circuit, and to meet time-to-market requirements, it is desirable to re-route only the ECO-affected portion of the circuit, while ...

3 (Special session) invited talks: selected European activities in SoC low power design methodologies and research networking: Fast, predictable and low energy memory references through architecture-aware compilation
Peter Marwedel, Lars Wehmeyer, Manish Verma, Stefan Steinke, Urs Helmig
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press
Full text available: pdf(233.00 KB) Publisher Site Additional Information: full citation, abstract, references

The design of future high-performance embedded systems is hampered by two problems: First, the required hardware needs more energy than is available from batteries. Second, current cache-based approaches for bridging the increasing speed gap between processors and memories cannot guarantee predictable real-time behavior. A contribution to solving both problems is made in this paper which describes a comprehensive set of algorithms that can be applied at design time in order to maximally exploit ...

4 An overview of the BlueGene/L Supercomputer

NR Adiga, G Almasi, GS Almasi, Y Aridor, R Barik, D Beece, R Bellofatto, G Bhanot, R Bickford, M Blumrich, AA Bright, J Brunheroto, C Caşcaval, J Castaños, W Chan, L Ceze, P Coteus, S Chatterjee, D Chen, G Chiu, TM Cipolla, P Crumley, KM Desai, A Deutsch, T Domany, MB Dombrowa, W Donath, M Eleftheriou, C Erway, J Esch, B Fitch, J Gagliano, A Gara, R Garg, R Germain, ME Giampapa, B Gopalsamy, J Gunnels, M Gupta, F Gustavson, S Hall, RA Haring, D Heidel, P Heidelberger, LM Herger, D Hoenicke, RD Jackson, T Jamal-Eddine, GV Kopcsay, E Krevat, MP Kurhekar, AP Lanzetta, D Lieber, LK Liu, M Lu, M Mendell, A Misra, Y Moatti, L Mok, JE Moreira, BJ Nathanson, M Newton, M Ohmacht, A Oliner, V Pandit, RB Pudota, R Rand, R Regan, B Rubin, A Ruehli, S Rus, RK Sahoo, A Sanomiya, E Schenfeld, M Sharma, E Shmueli, S Singh, P Song, V Srinivasan, BD Steinmacher-Burow, K Strauss, C Surovic, R Swetz, T Takken, RB Tremaine, M Tsao, AR Umamaheshwaran, P Verma, P Vranas, TJC Ward, M Wazlowski, W Barrett, C Engel, B Drehmel, B Hilgart, D Hill, F Kasemkhani, D Krolak, CT Li, T Liebsch, J Marcella, A Muff, A Okomo, M Rouse, A Schram, M Tubbs, G Ulsh, C Wait, J Wittrup, M Bae, K Dockser, L Kissel, MK Seager, JS Vetter, K Yates
November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Publisher: IEEE Computer Society Press
Full text available: pdf(357.61 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper gives an overview of the BlueGene/L Supercomputer. This is a jointly funded research partnership between IBM and the Lawrence Livermore National Laboratory as part of the United States Department of Energy ASCI Advanced Architecture Research Program. Application performance and scaling studies have recently been initiated with partners at a number of academic and government institutions, including the San Diego Supercomputer Center and the California Institute of Technology. This mass ...

5 Industry track session: Automated cleansing for spend analytics

Moninder Singh, Jayant R. Kalagnanam, Sudhir Verma, Amit J. Shah, Swaroop K. Chalasani
October 2005 **Proceedings of the 14th ACM international conference on Information and knowledge management CIKM '05**

Publisher: ACM Press
Full text available: pdf(490.93 KB) Additional Information: full citation, abstract, references, index terms

The development of an aggregate view of the procurement spend across an enterprise using transactional data is increasingly becoming a very important and strategic activity. Not only does it provide a complete and accurate picture of what the enterprise is buying and from whom, it also allows it to consolidate suppliers, as well as negotiate better prices. The importance, as well as the complexity, of this cleansing exercise is further magnified by the increasing popularity of Business Transform ...

Keywords: commodity mapping, information retrieval, knowledge management, spend analysis, unstructured data

6 Efficient declustering techniques for temporal access structures

Sanjiv Behl, Rakesh M. Verma
January 2001 **Proceedings of the 12th Australasian database conference ADC '01**
Publisher: IEEE Computer Society
Full text available: pdf(758.80 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

In this paper we address the problem of declustering temporal data and access structures for parallel architectures consisting of a single processor and multiple disks. To illustrate our techniques we choose the recently proposed Multi-Version Access Structure. We propose two new, efficient techniques called T-proximity and KT-proximity for assigning the data and index nodes of the multiversion access structure to multiple disks. The KT-proximity declustering technique considers both the key and ...

Keywords: access methods, declustering, parallelization, temporal databases

7 Application-specific architectures: Combining algorithm exploration with instruction set design: a case study in elliptic curve cryptography
Johann Großschädl, Paolo Ienne, Laura Pozzi, Stefan Tillich, Ajay K. Verma
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(232.20 KB) Additional Information: full citation, abstract, references

In recent years, processor customization has matured to become a trusted way of achieving high performance with limited cost/energy in embedded applications. In particular, Instruction Set Extensions (ISEs) have been proven very effective in many cases. A large body of work exists today on creating tools that can select efficient ISEs given an application source code: ISE automation is crucial for increasing the productivity of design teams. In this paper we show that an additional motivation fo ...

8 Industry track papers: A system for real-time competitive market intelligence
Sholom M. Weiss, Naval K. Verma
July 2002 **Proceedings of the eighth ACM SIGKDD international conference on Knowledge discovery and data mining**
Publisher: ACM Press
Full text available: pdf(1.16 MB) Additional Information: full citation, abstract, references, index terms

A method is described for real-time market intelligence and competitive analysis. News stories are collected online for a designated group of companies. The goal is to detect critical differences in the text written about a company versus the text for its competitors. A solution is found by mapping the task into a non-stationary text categorization model. The overall design consists of the following components: (a) a real-time crawler that monitors newswires for stories about the competitors (b) ...

9 Poster session: K-tree/forest: efficient indexes for boolean queries
Rakesh M. Verma, Sanjiv Behl
August 2002 **Proceedings of the 25th annual international ACM SIGIR conference on Research and development in information retrieval**
Publisher: ACM Press
Full text available: pdf(94.67 KB) Additional Information: full citation, abstract, references, index terms

In Information Retrieval it is well-known that the complexity of processing boolean queries depends on the size of the intermediate results, which could be huge (and are typically on disk) even though the size of the final result may be quite small. In the case of inverted files the most time consuming operation is the merging or intersection of the list of occurrences [1]. We propose, the Keyword tree (K-tree) and forest, efficient

structures to handle boolean queries in keyword-based informati ...

Keywords: indexing, keyword tree, keyword-based retrieval, parallelization

10 Spatio-temporal visualization of urban crimes on a GIS grid

Suresh K. Lodha, Arvind K. Verma
November 2000 **Proceedings of the 8th ACM international symposium on Advances in geographic information systems**
Publisher: ACM Press
Full text available: pdf(794.45 KB) Additional Information: full citation, abstract, index terms

We present several techniques for visualizing the temporal dimension of a Geographic Information System. Techniques include (i) pseudo-colored time-window display, (ii) side-by-side height bars, (iii) stacked time-aggregated cumulative bars, (iv) stacked order-preserving bus, (v) vertical time dimension, and (vi) multi-layered display. These techniques are presented in the context of an urban crime mapping application and extend the existing visualization techniques employed in this field. We ...

Keywords: GIS, spatio-temporal, urban crimes, visualization

11 Industry/government track posters: A system for automated mapping of bill-of-materials part numbers

Jayant Kalagnanam, Moninder Singh, Sudhir Verma, Michael Patek, Yuk Wah Wong
August 2004 **Proceedings of the tenth ACM SIGKDD international conference on Knowledge discovery and data mining KDD '04**
Publisher: ACM Press
Full text available: pdf(224.57 KB) Additional Information: full citation, abstract, references, index terms

Part numbers are widely used within an enterprise throughout the manufacturing process. The point of entry of such part numbers into this process is normally via a Bill of Materials, or BOM, sent by a contact manufacturer or supplier. Each line of the BOM provides information about one part such as the supplier part number, the BOM receiver's corresponding internal part number, an unstructured textual part description, the supplier name, etc. However, in a substantial number of cases, the BOM re ...

Keywords: bill of materials, data mining, part number mapping

12 Research track papers: Adversarial classification

Nilesh Dalvi, Pedro Domingos, Mausam, Sumit Sanghai, Deepak Verma
August 2004 **Proceedings of the tenth ACM SIGKDD international conference on Knowledge discovery and data mining KDD '04**
Publisher: ACM Press
Full text available: pdf(215.03 KB) Additional Information: full citation, abstract, references, citings, index terms

Essentially all data mining algorithms assume that the data-generating process is independent of the data miner's activities. However, in many domains, including spam detection, intrusion detection, fraud detection, surveillance and counter-terrorism, this is far from the case: the data is actively manipulated by an adversary seeking to make the classifier produce false negatives. In these domains, the performance of a classifier can degrade rapidly after it is deployed, as the adversary learns ...

Keywords: cost-sensitive learning, game theory, integer linear programming, naive Bayes, spam detection

13 Test and verification: An efficient control-oriented coverage metric

Shireesh Verma, Kiran Ramineni, Ian G. Harris

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(264.64 KB) Additional Information: full citation, abstract, references

Coverage metrics, which evaluate the ability of a test sequence to detect design faults, are essential to the validation process. A key source of difficulty in determining fault detection is that the control flow path traversed in the presence of a fault cannot be determined. Fault detection can only be accurately determined by exploring the set of all control flow paths, which may be traversed as a result of a fault. We present a coverage metric that determines the propagation of fault effects ...

14 Timing analysis and optimization: Crosstalk analysis using reconvergence correlation

Sachin Shrivastava, Rajendra Pratap, Harindranath Parameswaran, Manuj Verma

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press

Full text available: pdf(235.23 KB) Additional Information: full citation, abstract, references

In the UDSM era, crosstalk is an area of considerable concern for designers, as it can have a considerable impact on the yield, both in terms of functionality and operating frequency. Methods of crosstalk analysis are pessimistic in nature and the effort is ongoing to come up with techniques that make the analysis as realistic as possible. Using information from timing analysis is one such technique where we use data about overlap in switching among nets to identify those that can potentially sw ...

15 Controlling memory contention on a scalable multiprocessor-based telephone switch

Shikharesh Majumdar, Dale Streibel, Bruce Beninger, Brian Carroll, Neveenta Verma, Minru Liu

May 1999 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1999 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '99**, Volume 27 Issue 1

Publisher: ACM Press

Full text available: pdf(302.14 KB) Additional Information: full citation, index terms

16 Semantic web services: Meteor-s web service annotation framework

Abhijit A. Patil, Swapna A. Oundhakar, Amit P. Sheth, Kunal Verma

May 2004 **Proceedings of the 13th international conference on World Wide Web**

Publisher: ACM Press

Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, citings, index terms

The World Wide Web is emerging not only as an infrastructure for data, but also for a broader variety of resources that are increasingly being made available as Web services. Relevant current standards like UDDI, WSDL, and SOAP are in their fledgling years and form the basis of making Web services a workable and broadly adopted technology. However, realizing the fuller scope of the promise of Web services and associated service oriented architecture will requite further technological advances in ...

Keywords: ontology, semantic annotation of web services, semantic web services, web services discovery, wsdl

17 Advanced test solutions: Efficient on-line testing of FPGAs with provable diagnosabilities

Vinay Verma, Shantanu Dutt, Vishal Suthar

June 2004 **Proceedings of the 41st annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(335.66 KB) Additional Information: full citation, abstract, references, index terms

We present novel and efficient methods for on-line testing in FPGAs. The testing approach uses a ROving TEster (ROTE), which has provable diagnosabilities and is also faster than prior FPGA testing methods. We present 1- and 2-diagnosable built-in self-tester (BISTer) designs that make up the ROTE, and that avoid expensive adaptive diagnosis. To the best of our knowledge, this is the first time that a BISTer design with diagnosability greater than one has been developed for FPGAs. We also develo ...

Keywords: FPGAs, built-in self-tester (BISTer), diagnosability, functional testing, on-line testing, roving tester (ROTE)

18 Poster abstracts: Roving testing using new built-in-self-tester designs for FPGAs

Vinay Verma, Shantanu Dutt

February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Publisher: ACM Press

Additional Information: full citation, abstract

We propose a roving tester (ROTE) that tests the PLBs of the FPGA by periodically moving across it. At any time, the ROTE occupies a certain area of the FPGA, say two columns, and tests all PLBs in that area using parallel built-in self-tester (BISTers). A significant contribution of this work are designs for 1- and 2-diagnosable BISTers. To the best of our knowledge, this is the first time that BISTer designs with provable diagnosabilities have been developed for FPGAs. We also develop function ...

19 Provisioning: On admission control for profit maximization of networked service providers

Akshat Verma, Sugata Ghosal

May 2003 **Proceedings of the 12th international conference on World Wide Web**

Publisher: ACM Press

Full text available: pdf(234.25 KB) Additional Information: full citation, abstract, references, citings, index terms

Variability and diverseness among incoming requests to a service hosted on a finite capacity resource necessitates sophisticated request admission control techniques for providing guaranteed quality of service (QoS). We propose in this paper a service time based online admission control methodology for maximizing profits of a service provider. The proposed methodology chooses a subset of incoming requests such that the revenue of the provider is maximized. Admission control decision in our propo ...

Keywords: admission control, profit maximization, quality of service (QoS), service level agreement (SLA), service time estimation, short-term prediction, shortest remaining job first (SRJF), web service

20 Experiences with a mobile robotic guide for the elderly

Michael Montemerlo, Joelle Pineau, Nicholas Roy, Sebastian Thrun, Vandi Verma

July 2002 **Eighteenth national conference on Artificial intelligence**
Publisher: American Association for Artificial Intelligence
Additional Information: full citation, abstract, references, citings, index terms

This paper describes an implemented robot system, which relies heavily on probabilistic AI techniques for acting under uncertainty. The robot Pearl and its predecessor Flo have been developed by a multi-disciplinary team of researchers over the past three years. The goal of this research is to investigate the feasibility of assisting elderly people with cognitive and physical activity limitations through interactive robotic devices, thereby improving ...

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Relevance scale

1 Constructing 1-writer multireader multivalued atomic variables from regular variables
S. Haldar, K. Vidyasankar
January 1995 **Journal of the ACM (JACM)**, Volume 42 Issue 1
Publisher: ACM Press
Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

A simple wait-free construction of 1-writer multireader multivalued atomic variable from multireader regular variables is presented in this paper. A key point of the construction is the use of an elegant forwarding technique to overcome the new-old inversion property inherent in regular variables.Another construction, using a different forwarding technique, is also given. This technique is a refinement of one proposed in the literature.Formal correctness proofs for bot ...

Keywords: nonatomic operation execution, reader and writer, regular and atomic, shared variable-safe, wait-freedom

2 Session 1: Tool support for randomized unit testing
James H. Andrews, Susmita Haldar, Yong Lei, Felix Chun Hang Li
July 2006 **Proceedings of the 1st international workshop on Random testing RT '06**
Publisher: ACM Press
Full text available: pdf(336.44 KB) Additional Information: full citation, abstract, references, index terms

There are several problem areas that must be addressed when applying randomization to unit testing. As yet no general, fully automated solution that works for all units has been proposed. We therefore have developed RUTE-J, a Java package intended to help programmers do randomized unit testing in Java. In this paper, we describe RUTE-J and illustrate how it supports the development of per-unit solutions for the problems of randomized unit testing. We report on an experiment in which we applied R ...

Keywords: randomized testing, unit testing

3 DataBlitz storage manager: main-memory database performance for critical applications
J. Baulier, P. Bohannon, S. Gogate, C. Gupta, S. Haldar
June 1999 **ACM SIGMOD Record , Proceedings of the 1999 ACM SIGMOD international**

conference on Management of data SIGMOD '99, Volume 28 Issue 2
Publisher: ACM Press
Full text available: pdf(227.43 KB) Additional Information: full citation, references, citings, index terms

4 Bounded concurrent timestamp systems using vector clocks
Sibsankar Haldar, Paul Vitányi
January 2002 **Journal of the ACM (JACM)**, Volume 49 Issue 1
Publisher: ACM Press
Full text available: pdf(330.18 KB) Additional Information: full citation, abstract, references, citings, index terms

Shared registers are basic objects used as communication mediums in asynchronous concurrent computation. A concurrent timestamp system is a higher typed communication object, and has been shown to be a powerful tool to solve many concurrency control problems. It has turned out to be possible to construct such higher typed objects from primitive lower typed ones. The next step is to find efficient constructions. We propose a very efficient wait-free construction of bounded concurrent timestamp sy ...

Keywords: Concurrent reading while writing, label, labeling and scan, nonatomic operation execution, operation execution, operation---read and write, regular and atomic, shared variable---safe, timestamp system, traceability, vector clock, wait-freedom

5 Space-efficient construction of buffer-optimal 1-writer 1-reader multivalued atomic variable
S. Haldar, K. Vidyasankar
May 1996 **Proceedings of the fifteenth annual ACM symposium on Principles of distributed computing**
Publisher: ACM Press
Full text available: pdf(97.82 KB) Additional Information: full citation, references, index terms

6 Poster session: Making area-performance tradeoffs at the high level using the AccelFPGA compiler for FPGAs
P. Banerjee, V. Saxena, J. Uribe, M. Haldar, A. Nayak, V. Kim, D. Bagchi, S. Pal, N. Tripathi, R. Anderson
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Applications such as digital cell phones, 3G wireless receivers, and voice over IP, require DSP functions that are typically mapped onto general purpose DSP processors. With the introduction of advanced FPGA architectures which provide built-in DSP support such as the Xilinx Virtex-II, and the Altera Stratix, a new hardware alternative is available for DSP designers. DSP design has traditionally been divided into algorithm development and hardware/software implementation. The majority of DSP alg ...

7 An efficient solution to the mutual exclusion problem using unfair and weak semaphore
S. Haldar, D. Subramanian
April 1988 **ACM SIGOPS Operating Systems Review**, Volume 22 Issue 2
Publisher: ACM Press

Full text available: pdf(509.53 KB) Additional Information: full citation, index terms

8 Fairness in processor scheduling in time sharing systems



S. Haldar, D. K. Subramanian

January 1991 **ACM SIGOPS Operating Systems Review**, Volume 25 Issue 1

Publisher: ACM Press

Full text available: pdf(852.91 KB) Additional Information: full citation, abstract, citings, index terms

Loosely, fairness is the assurance of granting each request, from a set of requests, within a predetermined bounded time even though the request scheduling primitives are unfair or random. The fairness property has been studied, in solutions to the mutual exclusion problem, from theoretical point of view. Many fair solutions to the mutual exclusion problem have been proposed in recent years. This paper presents one illustration to show how the concepts of fairness could be incorporated in proces ...

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